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Claims

[c0001] 1. A semiconductor device integrated a triple well structure and a bonding pad structure, said semiconductor device integrated a triple well structure and a bonding pad structure comprising:
a substrate having a triple well structure therein, said triple well structure comprising a doped region of a conductive type, a first well region of a first conductive type below said doped region, and a second well region of a second conductive type below said first well region; and
a bonding pad structure on said substrate.

[c0002] 2. The semiconductor device integrated a triple well structure and a bonding pad structure according to claim 1, wherein a dopant concentration of said second well region of said second conductive type is higher than a dopant concentration of said first well region of said first conductive type.

[c0003] 3. The semiconductor device integrated a triple well structure and a bonding pad structure according to claim 1, wherein said first conductive type is opposite to said second conductive type.

[c0004] 4. The semiconductor device integrated a triple well structure and a bonding pad structure according to claim 1, wherein said dopant concentration of said first well region of said second conductive type is higher than a dopant concentration of said doped region.

[c0005] 5. The semiconductor device integrated a triple well structure and a bonding pad structure according to claim 1, wherein said bonding pad structure comprises:
a multiple metal layers alternating stacked with a multiple dielectric layers on said substrate; and
a top metal layer on said multiple metal layers.

[c0006] 6. The semiconductor device integrated a triple well structure and a bonding pad structure according to claim 5, wherein said each of said multiple metal layers coupled with adjacent said each of said multiple metal layers by a plurality of via plugs in each of said multiple dielectric layers.

[c0007] 7. The semiconductor device integrated a triple well structure and a bonding pad structure according to claim 1, further comprising a passivation layer with a bonding pad opening on said bonding pad structure.

[c0008] 8. A semiconductor device with a low capacitance bonding pad structure therein, said semiconductor device

with a low capacitance bonding pad structure comprising:

a substrate having a doped region of a conductive type therein;

a first well region of a first conductive type in said substrate, and below said doped region;

a second well region of a second conductive type in said substrate, and below said doped region and said first well region;

a multiple metal layers alternating with a multiple dielectric layers on said substrate, wherein said multiple metal layers are buried deeply in said multiple dielectric layers;

a top metal layer on said multiple metal layers; and

a passivation layer with an bonding pad opening therein on said top metal layer.

[c0009] 9. The semiconductor device with a low capacitance bonding pad structure according to claim 8, wherein said first conductive type is opposite to said second conductive type.

[c0010] 10. The semiconductor device with a low capacitance bonding pad structure according to claim 8, wherein a dopant concentration of said second well region of said second conductive type is higher than a dopant concentration of said first well region of said first conductive type.

[c0011] 11. The semiconductor device with a low capacitance bonding pad structure according to claim 8, wherein a dopant concentration of said first well region of said first conductive type is higher than a dopant concentration of said first doped region of said second conductive type.

[c0012] 12. The semiconductor device with a low capacitance bonding pad structure according to claim 8, wherein each of said multiple metal layers coupled with adjacent each said multiple metal layers by a plurality of via plugs in each of said multiple dielectric layers.